Docket No.: 071971-0015 **PATENT**

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of	:	Customer Number: 53080
Shiro SAKIYAMA, et al.	:	Confirmation Number: 6689
Patent No.: 7,498,865	:	Issue Date: March 3, 2009
Application No.: 10/511,165	:	Group Art Unit: 2816
Filed: October 14, 2004	:	Examiner: HILTUNEN, THOMAS J

For: SEMICONDUCTOR INTEGRATED CIRCUIT WITH REDUCED SPEED VARIATIONS

REQUEST FOR CERTIFICATE OF CORRECTION UNDER 37 CFR 1.322

Mail Stop Certificate of Correction
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

In reviewing the above-identified patent, a printing error was discovered therein requiring correction in order to conform the Official Record in the application.

The error noted is set forth on the two attached copies of form PTO-1050 Rev. 2-93 in the manner required by the Commissioner's Notice.

Specifically, On the title page, in Item "(75) Inventors", change the cities of residence for the three inventors from "Shiro Sakiyama, Yawata (JP)" to --Shiro Sakiyama, Kyoto (JP)--; from "Masayoshi Kinoshita, Settsu (JP)" to --Masayoshi Kinoshita, Osaka (JP)--; and from "Masaya Sumita, Amagasaki (JP)" to --Masaya Sumita, Hyogo (JP)--. Also, in Item "(87) PCT Pub. Date:", change "Oct. 9, 2004" to --September 10, 2004--. Attached are copies of the Declaration which indicates the correct addresses for the inventors and a copy of the front page

of published application WO 2004/077673 which indicates the publication date as September 10, 2004.

The change requested herein occurred as a result of printing the Letters Patent and the Certificate should be issued without expense under Rule 322 of the Rules of Practice. Accordingly, Applicants request issuance of the Certificate of Correction.

Please charge any shortage in fees due in connection with the filing of this paper to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

MCDERMOTT WILL & EMERY LLP

Michael E. Fogarty
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Please recognize our Customer No. 53080 as our correspondence address.

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WDC99 1727045-1.071971.0015

UNITED STATES PATENT AND TRADEMARK OFFICE
CERTIFICATE OF CORRECTION

PATENT NO : 7,498,865 Page 1 of 1

APPLICATION NO. : 10/511,165

ISSUE DATE : March 03, 2009

INVENTOR(S) : Shiro SAKIYAMA, et al.

It is certified that an error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

On the title page, in Item "(75) Inventors", change the cities of residence for the three inventors as follows:

"Shiro Sakiyama, Yawata (JP)" to --Shiro Sakiyama, Kyoto (JP)--;
"Masayoshi Kinoshita, Settsu (JP)" to --Masayoshi Kinoshita, Osaka (JP)--;
"Masaya Sumita, Amagasaki (JP)" to --Masaya Sumita, Hyogo (JP)--.; and

In Item "(87) PCT Pub. Date:", change "Oct. 9, 2004" to --September 10, 2004--.

MAILING ADDRESS OF SENDER (Please do not use customer number below):

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(12)特許協力条約に基づいて公開された国際出願

(19) 世界知的所有権機関
国際事務局

(43) 国際公開日
2004年9月10日 (10.09.2004)

PCT

(10) 国際公開番号
WO 2004/077673 A1

(51) 国際特許分類7: **H03K 17/687**, 19/094, H01L 27/088

(21) 国際出願番号: PCT/JP2004/001942

(22) 国際出願日: 2004年2月19日 (19.02.2004)

(25) 国際出願の言語: 日本語

(26) 国際公開の言語: 日本語

(30) 優先権データ:
特願2003-047418 2003年2月25日 (25.02.2003) JP

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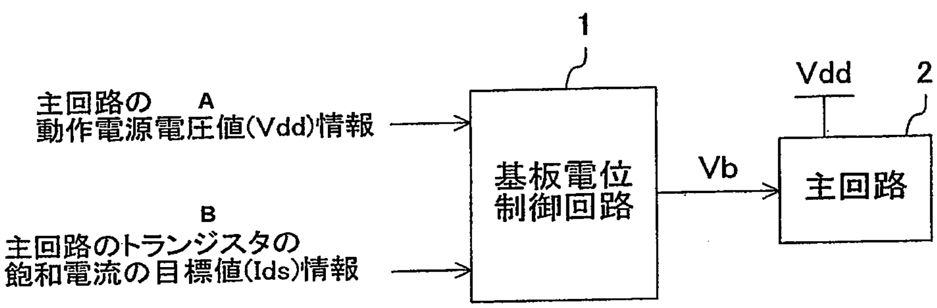
(81) 指定国 (表示のない限り、全ての種類の国内保護が可能): AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BW, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NA, NI, NO, NZ, OM, PG, PH, PL, PT, RO, RU, SC, SD, SE, SG, SK, SL, SY, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, YU, ZA, ZM, ZW.

(84) 指定国 (表示のない限り、全ての種類の広域保護が可能): ARIPO (BW, GH, GM, KE, LS, MW, MZ, SD, SL, SZ, TZ, UG, ZM, ZW), ユーラシア (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), ヨーロッパ (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HU, IE, IT, LU,

[続葉有]

(54) Title: SEMICONDUCTOR INTEGRATED CIRCUIT

(54) 発明の名称: 半導体集積回路



A...INFORMATION CONCERNING OPERATING POWER SUPPLY VOLTAGE (Vdd) OF MAIN CIRCUIT
B...INFORMATION CONCERNING TARGET SATURATION CURRENT VALUE (Ids) OF TRANSISTOR OF MAIN CIRCUIT
1...SUBSTRATE POTENTIAL CONTROLLING CIRCUIT
2...MAIN CIRCUIT

(57) **Abstract:** A semiconductor integrated circuit comprises a main circuit (2) which is composed of a MOS transistor wherein a source and a substrate are separated from each other. A substrate potential controlling circuit (1) controls the substrate potential of the MOS transistor of the main circuit (2) so that the actual saturation current value of the MOS transistor which constitutes the main circuit (2) becomes equal to a target saturation current value (Ids) of the main circuit (2) at the operating power supply voltage (Vdd). Consequently, even when the operating power supply voltage of the semiconductor integrated circuit is lowered, variations in the operating speed can be suppressed within a small range.

[続葉有]

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Docket No. ___________

COMBINED DECLARATION/POWER OF ATTORNEY
FOR PATENT APPLICATION

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name.

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled SEMICONDUCTOR INTEGRATED CIRCUIT ______________________, the specification of which

(check one) ___ is attached hereto.

___ was filed on ______________________ as Application Serial No. ______________.

X PCT International Patent Application Number **PCT/JP2004/001942** filed on **February 19, 2004** and was amended on ______________ (if applicable).

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose information which is material to the examination of this application in accordance with Title 37, Code of Federal Regulations, § 1.56(a).

I hereby claim foreign priority benefits under Title 35, United States Code, § 119 of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed:

Prior Foreign Application(s)			Priority Claimed
2003-047418 (Number)	JAPAN (Country)	25/02/2003 (Day/Month/Year Filed)	X Yes ___ No
(Number)	(Country)	(Day/Month/Year Filed)	___ Yes ___ No
(Number)	(Country)	(Day/Month/Year Filed)	___ Yes ___ No

I hereby claim the benefit under Title 35, United States Code, § 120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, § 112, I acknowledge the duty to disclose material information as defined in Title 37, Code of Federal Regulations, § 1.56(a) which occurred between the filing date of the prior application and the national or PCT international filing date of this application:

(Appln. Serial No.)	(Filing Date)	(Status-patented, pending, abandoned)
(Appln. Serial No.)	(Filing Date)	(Status-patented, pending, abandoned)

I hereby appoint as my attorneys, with full power of substitution and revocation, to prosecute the patent application identified above and to transact all business in the U.S. Patent and Trademark Office connected therewith: Raphael V. Lupo (Reg. No. 28,363); Jack Q. Lever, Jr. (Reg. No. 28,149); Kenneth L. Cage (Reg. No. 26,151); Stanislaus Aksman (Reg. No. 28,562); Michael E. Fogarty (Reg. No. 36,139); Brian E. Ferguson (Reg. No. 36,801); Robert W. Zelnick (Reg. No. 36,976); Edward E. Kubasiewicz (Reg. No. 30,020); Paul Devinsky (Reg. No. 28,553); and Wilhlem F. Gadiano (Reg. No. 37,136); Laura A. Donnelly (Reg. No. 38,435); Craig L. Plastrik (Reg. No. 41,254), David A. Spenard (Reg. No. 37,449)

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I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

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Inventor's signature Shiro SAKIYAMA Date October 7, 2004

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